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| **Digital circuits laboratory class** | **Year 2024, exercise 4** |
| Author: Jakub Turkowski | Title of the exercise: Analysis of synchronous circuit |
| Laboratory group number: 2 | Week day: Tuesday  Realization date: 09.04.2024  Hours of the lab: 15:15-16:55 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| X | D1 | D1 NEXT | D2 | D2 NEXT | Y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Obraz zawierający diagram, Plan, tekst, linia

Opis wygenerowany automatycznie

As the first row of NAND gate of a JK flipflop additionally takes in the output (regular and negated) it kind makes the gates of the circuit with D flipflop obsolete. For it to reset however we need to take into account the change of clock and value of X, which will be inserted using the and gate.

Obraz zawierający diagram, tekst, linia, Plan

Opis wygenerowany automatycznie

Obraz zawierający diagram, tekst, Plan, linia

Opis wygenerowany automatycznie

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| time | t1 | t2 | t3 | t4 | t5 | t6 |
| x | 1 | 1 | 1 | 1 | 0 | 0 |
| y1y2 | 1 0 | 0 1 | 1 1 | 1 1 | 0 0 | 0 0 |
| Z | 0 | 0 | 1 | 1 | 0 | 0 |

For the NAND version:

D1: (y1’x)+(y2x) = ((y1’x)’(y2x)’)’

D2: (y1x)+(y2x) = ((y1x)’(y2x)’)’

O: (y2y1) = ((y2y1)’)’